UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,715	03/29/2004	Tom Gong Lei	1459-CA (P283US)	1443

7590 11/19/2007

James J. Murphy
P.O. Box 50784
Dallas, TX 75201

EXAMINER	
LAUTURE, JOSEPH J	
ART UNIT	PAPER NUMBER
2819	
MAIL DATE	DELIVERY MODE
11/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/811,715	LEI ET AL.	
	Examiner	Art Unit	
	Joseph Lauture	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-18,25 and 26* is/are allowed.

6)☐ Claim(s) *1,2,4,6-8 and 19-24* is/are rejected.

7)☒ Claim(s) *3,5 and 9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The application has not been checked to the extent necessary to determine the presence of all possible typographical and grammatical errors. Applicant's cooperation is requested in correcting any errors of which he/she may become aware in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 6-8 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Melanson et al (US 6,670,902) in view of Batra et al (US 6,985,532).

Regarding claim 1, Melanson et al teach in figure (3A) a delta sigma modulator apparatus and method, the apparatus comprising: a first element/unit made of switches (301a, 301b, 320a, 302b) used for sampling noise from and discharging noise to a signal line (V_{IN+}, V_{IN-}) in response to an inherent control signal using a capacitor (303a), the noise included in the input signal; a second unit/element made of switches (301c, 301d, 302c, 302d) used for sampling noise from and discharging noise to the signal line (V_{IN+}, V_{IN-}) in response to an inherent control signal using a capacitor (303b), wherein the sampling and discharging frequency of the switches is inherently independent of the input signals.

Melanson et al does not specifically teach that the control signal that triggers the sampling and discharging of noise is in response to an input signal transitioning on selected edges (falling or rising) of a clock signal. However, such schemes are well known in the art, as evidenced by Batra et al. Batra et al disclose a transmitter system and method wherein they teach that a control signal can be specified by selected edges of a clock signal (See column 10, lines 55-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Melanson et al and of Batra et al to realize a circuit having improved performance and reliability because that would allow the generation of pulses having varying duration, magnitude and type to meet changing needs of modulation schemes (See column 2, lines 64-67).

Regarding claim 7, Melanson et al teach in figure (3A) a delta sigma modulator apparatus and method, the method comprising: using a first element/unit made of switches (301a, 301b, 320a, 302b) for sampling noise from and discharging noise to a signal line (V_{IN+}, V_{IN-}) in response to an inherent control signal using a capacitor (303a), the noise included in the input signal; using a second unit/element made of switches (301c, 301d, 302c, 302d) for sampling noise from and discharging noise to the signal line (V_{IN+}, V_{IN-}) using a capacitor (303b), in response to an inherent control signal, wherein the sampling and discharging frequency of the switches is inherently independent of the input signals.

Melanson et al does not specifically teach that the control signal that triggers the sampling and discharging of noise is in response to an input signal transitioning on

selected edges (falling or rising) of a clock signal. However, such schemes are well known in the art, as evidenced by Batra et al. Batra et al disclose a transmitter system and method wherein they teach that a control signal can be specified by selected edges of a clock signal (See column 10, lines 55-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Melanson et al and of Batra et al to realize a circuit having improved performance and reliability because that would allow the generation of pulses having varying duration, magnitude and type to meet changing needs of modulation schemes (See column 2, lines 64-67).

Regarding claim 19, Melanson et al teach in figure (3A) a delta sigma modulator apparatus and method, the method comprising: using a set of switches (301a, 301b, 320a, 302b) to couple a node (A) to a signal line (V_{IN+}, V_{IN-}) in response to an inherent control signal to sample and discharge noise from and to using a capacitor (303a); using a set of switches (301c, 301d, 302c, 302d) to couple a matching node (B) to the signal line (V_{IN+}, V_{IN-}) in response to an inherent control signal to sample and discharge noise from and to the signal line using a capacitor (303b), at a frequency that inherently relates to the clock signal.

Melanson et al does not specifically teach that the control signal that triggers the coupling of the nodes is in response to an input signal transitioning on selected edges (falling or rising) of a clock signal. However, such schemes are well known in the art, as evidenced by Batra et al. Batra et al disclose a transmitter system and method wherein they teach that a control signal can be specified by selected edges of a clock signal

(See column 10, lines 55-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Melanson et al and of Batra et al to realize a circuit having improved performance and reliability because that would allow the generation of pulses having varying duration, magnitude and type to meet changing needs of modulation schemes (See column 2, lines 64-67).

Regarding claims 2, 4, 6, 8, 20 and 21, Melanson teaches in figure (3A): an operational amplifier (312) having an input coupled to the signal line, the signal line being coupled to a first data conversion element made of switches (301a, 301b, 320a, 302b) through a first node and to a dummy conversion element made of switches (301c, 301d, 302c, 302d) matching the first data conversion element through a second node in response to an input signal, wherein the sampling and discharging frequency on the signal line inherently relates to a frequency of the clock signal.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over McMahon (US 4,208,651) in view of Dedic (US 6,344,816).

Regarding claim 22, McMahon teaches in figure (18) a circuit comprising: a first set of shift register elements (290) associated with a first load (294) which may include more than one buffer/load units, the first set of shift registers presenting data on a corresponding signal line in response to a first input signal (D1); a second set of shift registers (293) associated with a second load (295) which may include more than one buffer/load units, the second set of shift registers presenting data on the signal line in response to a second input signal (D3).

McMahon does not teach a circuit wherein a system loading is independent of the first and second input signals. However, such schemes are known in the art, as evidenced by Dedic. Dedic discloses a mixed-signal circuit wherein the system loading is independent any input signal (See column 11, lines 43-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of McMahon and of Dedic to realize a circuit having improved performance and reliability because that would significantly reduce data-dependent jitter (See column 3, lines 19-20).

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over McMahon (US 4,208,651) in view of Dedic (US 6,344,816) and further in view of Osamura et al (US 7,049,879).

Regarding these claims, the combination of McMahon and Dedic teaches the essential features of the claimed invention as set forth above, except for the step of loading on a substrate and loading on a power supply. Osamura et al teach a power supply circuit and method, the method including the steps of loading on a substrate and loading on a power supply (See column 5, lines 33-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of McMahon, of Dedic and of Osamura et al to realize a system having improved performance and reliability because that would allow an improved rise characteristic of the output voltage (See column 2, lines 25-27).

Allowable Subject Matter

Claims 3, 5 and 9-11are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12-18, 25 and 26 are allowable.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Lauture, whose telephone number is (571) 272-1805. The examiner can normally be reached Monday to Friday between 9:30 am and 6:00 PM

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached at (571) 272-7492. The fax number for the organization to which this application is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov.*** Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free). For assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joseph Lauture
Art Unit: 2819
Date: 11/08/2007